1. (Twice Amended) A method, comprising:

B1

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material;

Pub C1

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

B2

2. (Amended) The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. (Amended) The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said series of relatively narrow trenches and said relatively wide trench.

B3

10. (Amended) The method of claim 9, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

Pub C4

11. (Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said trench and said series of trenches.

17. (Twice Amended) A substantially planar semiconductor topography, comprising:

B4

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

Pub C6

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and